Amendments to the Specification:

Please replace the paragraph beginning on page 7, line 3 with the following amended paragraph:

The inventive techniques disclosed herein are applicable to several types of digital circuitry. By way of one exemplary embodiment, the inventive techniques for producing digital circuitry ~~will discuss the techniques~~ are disclosed within the context of one type of digital ~~circuitry,~~ circuitry: large area line conductive pads. Large area line conductive pads are typically used for interconnection of stackable circuitry in a Permanent Inexpensive, Rugged Memory (PIRM) cross-point memory arrays, can be produced according to different methods of lithography, and in one preferred embodiment, can be fabricated on a plastic web based roll to roll environment according to an improved emboss and lift technique are disclosed in U.S. Application No. 10/244,862, entitled "Embossed Mask Lithography," ~~U.S. Application No. ######## (Attorney Docket No. 10003812, titled "Embossed Mask Lithography"),~~ the disclosure of which is hereby incorporated by reference. In the following description, for purposes of explanation, specific nomenclature and specific implementation details are set forth to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that these specific details are not necessarily required in order to practice the present invention.

Please replace the paragraph beginning on page 9, line 17 with the following amended paragraph:

When manufacturing PIRM memory layers for digital memory systems, interconnection or conductive pads are often required on the end of electrodes in stackable circuitry. This is because a typical PIRM memory module is formed of a plurality of layers each having a cross-point memory array. Many layers can be stacked to form a single memory module, allowing the

memory module to have a storage capacity of many multiples of the data storage possible on a single layer. Construction of a PIRM memory module therefore involves the stacking of multiple layers of memory into an interconnected three-dimensional storage module. U.S. patent application Ser. No. 09/875,356, entitled "Non-Volatile Memory," ~~U.S. patent application Ser. No. ####### (Attorney Docket No.10002367)~~ details the technology involved in providing the improved stackable circuitry in PIRM memory modules as referenced throughout, while U.S. patent application Ser. No. 09/875,833, entitled "Digital Camera Memory System," ~~U.S. patent application Ser. No. ####### (Attorney Docket No. 10003477)~~ details the generally referenced PIRM based digital memory systems for consumer devices. The disclosures of both documents are explicitly incorporated herein by reference. Conductive pads are found within PIRM memory modules where both the stackable circuitry and the conductive pads are produced using simple and inexpensive processing. Through use of a flexible plastic or metal substrate, roll to roll processing is possible in fabrication of the circuits on the layers. Conductive pads are thereby formed on the substrate for the making of external connection to the various layers of stackable circuits. A plurality of the layers are stacked on top of one another and laminated together. The memory module is then completed by forming and pattering external contact tracks ~~which~~ that make electrical contact with the conductive pads at the edges of the memory module layers.

Please replace the paragraph beginning on page 10, line 24 with the following amended paragraph:

For example, in non-lift off based processes, such as those described in U.S. patent application Ser. No. 10/058,744, entitled "Optical-Mechanical Feature Fabrication During Manufacture Of Semiconductors And Other Micro-Devices and Nano-Devices That Include Micron And Sub-Micron Features," ~~U.S. patent application Ser. No. ####### (Attorney Docket No. 100019855)~~, the specification of which is hereby incorporated by reference, embossing a

pattern with large features and small features is difficult because of "capillary" action whereby an applied polymer is wicked into the small (narrow) feature areas, thereby starving the large feature areas of the needed polymer. The practical result of this uneven polymer settlement is that the smaller (narrower) areas may have a higher polymer profile compared to the wider areas. Similarly, ~~lift off based processes~~ in lift off based processes, embossing a pattern with large features (e.g., a wide area) is problematic because the pressure sensitive adhesives which are typically used in the lift off step may adhere not to only the peaks, but may also sag into the trenches, thereby inadvertently adhering to and removing desired depositions from the trench floor. Given the described maximum feature size limitation on the different embossing procedures, there is a need to apply the inventive concept of waffling to all of the various embossing processes, whether lift off or non-lift off based.